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A Study on Multi Material Gate All Around SOI MOSFET

Neeraj Gupta
Lecturer, Amity School of Engineering & Technology,
Amity University, Haryana, India

A.K. Raghav
Director, IRD,
Amity University, Haryana, India

Alok K. Kushwaha
Professor., Birla Institute of Technology & Science, Dubai, UAE

Abstract— **As the continuous down scaling of MOSFET device is required to increase the speed and packaging density of it, but it reduces the device characteristics in terms of short channel effect and reverse leakage current. At present, the single gate MOSFET reaching its scaling limit. These limitations associated with scaling give birth to number of innovative techniques which includes the use of different device structures, different channel materials and different gate oxide materials. In this paper different short channel effects suggested by different authors are covered along with their method of minimization. A structure based on the Fully depleted SOI Gate all around MOSFET has been suggested to overcome the scaling limit.**

Keywords- SCE; SOI; DIBL; Multigate and S.

I. INTRODUCTION

CMOS technology has contributed efficiently for the development of almost all the countries. This is due to the vast applications of CMOS. As the technology changes rapidly corresponding consumer electronic device requirements are also growing. The semiconductor industry maintains a "roadmap", the ITRS [1], which sets the pace for MOSFET growth. The latest Itanium-7 quad core GPU processor contains more 1.1 billion transistors in a 160 mm² chip area and Intel 32 nm SRAM wafer (1Tb) has about 800 billion transistors [2]. Device engineers all over the world have made this speculate come true through a magic named "Scaling". The scaling based MOSFET replace the bulk CMOS and will make the computer-era faster and more reliable. It will bring revolution in the world of communication and electronics, as everything is digitalized and depends on transistors. Even a small digital clock needs timer circuits for its operation and also a computer processor, RAM etc.; they too need transistor for operation. Scaling has also enhanced the cut-off frequency making this technology attractive for System- On-Chip (SOC) applications where both analog and digital circuits are realized on the same chip for reduced cost and better performance.SOI microprocessors with a 22% speed improvement over bulk have been reported recently [1]. Fully depleted MOSFETs with a gate length of 50 nm and a switching speed less than a picosecond [2] have been reported.

The integrated circuit performance increases exponentially with the scaling of MOSFET (Metal oxide field effect transistor) dimensions. While on the other side, the scaling of MOSFET dimensions leads to the close proximity between source and drain electrode and it decrease the control of gate electrode and also causes short channel effect. First of all was excessive heating effect produced in the circuits. Furthermore they showed a large number of short channel effects which badly affected the performance. Scaling trend in CMOS approaching physical limits prompts the need for alternative device.

To overcome this limitation a large number of new device structures have been proposed. One of such device structures is gate all around MOSFET that is important for many applications point of view such as SRAM for ultra low power . The gate all around (GAA) MOSFET with proper design parameters are attractive for circuit design in nanometer era because of better scalability. The GAA MOSFETs are used for low voltage, low power and high frequency applications.

In this review paper, there are four sections. Section I includes the introduction , Section II described different problems occurred during scaling of MOSFET , Section III covered solution of those problem occurred during scaling and Section IV includes the proposed work on the basis of section III solution.

II. SHORT CHANNEL EFFECTS

Gordon Moore made an empirical observation in 1965 that the number of devices on a chip doubles every 18 or 24 months[3]. Following Moore law various MOSFET models designed. As the CMOS technology scaling enters the nanometer regime, many serious problems called the small geometry effects or short channel effects(SCEs) comes into play. Some of these effects are such as increased leakage currents, difficulty on increase of on-current, large parameter variations, low reliability and yield, increase in manufacturing cost, and etc. Hence there is a need of considering the new device structures with new gate materials and new dielectric to suppressed the short channel effects.

A. DIBL(Drain Induced Barrier Lowering)

Drain induced barrier lowering is a short channel effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. As drain

voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device. In effect, the channel becomes more attractive for electrons. In other words, the potential energy barrier for electrons in the channel is lowered. Hence the term "barrier lowering" is used to describe these phenomena. It can be minimized by increasing the doping concentration of the channel region [4,8].

B. *Surface scattering*

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering causes reduction of the mobility, the electrons move with great difficulty parallel to the interface.

C. *Velocity saturation*

The performance of short-channel devices are also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low E_y, the electron drift velocity V_{de} in the channel varies linearly with the electric field intensity. Note that the drain current is limited by velocity saturation instead of pinchoff. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages[5].

D. *Impact ionization*

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization. It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 6V, the normally reversed-biased substrate-source pn junction will conduct appreciably. They can gain enough energy as they travel toward the drain to create new eh pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip[6].

E. *Hot electrons*

Another problem, related to high electric fields, is caused by so-called hot electrons. These high energy electrons can enter the oxide, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_{th} and affect adversely the gate's control on the drain current[7].

F. *Threshold Voltage Roll-off*

Since the threshold voltage (*Vth*) is directly related to the device speed and sub-threshold leakage current, it has to be minimized. It is generally expressed in terms of a *Vth* roll-off. The transistors with a different channel length (L) in the same wafer, even in the same die, yield different *Vth*. The threshold voltage reduction due to the reduced channel length represents *Vth* roll-off[8].

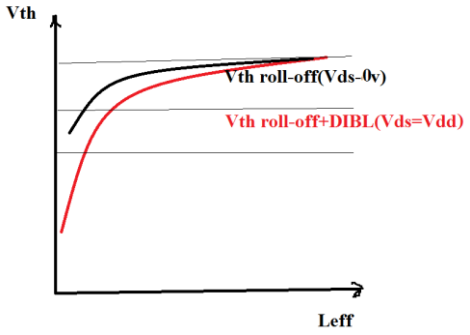

Figure 1. Threshold voltage roll-off and drain induced barrier lowering (DIBL).

G. *Sub-threshold leakage current*

The Sub-threshold leakage current is the weak inversion conduction current, which is dominated by the diffusion current flowing between the drain and source when |V*GS*|<|V*th*|. It is considered as one of non-ideal characteristics of MOSFET as a switching device and contributes major portions of the standby leakage power dissipation[9]. This weak inversion conduction current I_{subth} can be expressed based on the Eq. given below

$$= \mu C_{dep} \left(\frac{W}{l}\right) V_T{}^2 \left(\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\right) \left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

Isubth increases exponentially with both increasing *VGS* and decreasing *Vth*, the partial derivative of *log*10*Isubth* with respect to *VGS* yields a constant slope called sub-threshold slope (SS) and equals to

$$SS = \frac{\partial(Log_{10} I_{subth})}{\partial V_{GS}}$$

$$== \frac{1}{Ln\ 10\ .I_{subth}}\ X \frac{\partial I_{subth}}{\partial V_{GS}}$$

In order to turn off the transistor effectively, SS must be designed to be as small as possible. Figure 2.1 [10,15] shows that SS is always greater than 2.3 VT (60 mV/dec) at room temperature and shows how well the channel surface potential can be controlled by the gate contact. SS can be made smaller y using a thinner gate oxide thickness.

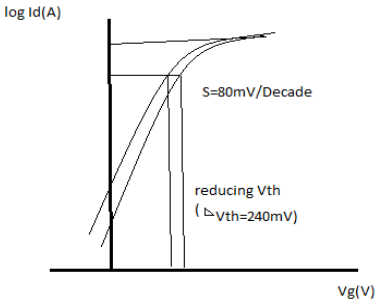

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Figure 2. Characteristics of sub-threshold conduction.

For MOS a transistor built in SOI technology, the sub-threshold swing is usually better than in bulk technology This

makes SOI a promising candidate for ultra low power CMOS applications [9].

H. Punchthrough

When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge, punchthrough occurs. Punchthrough can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels[11].

I. Channel Length Modulation

As the channel length decreases then the effect of drain to source voltage as well as the gate to source voltage affects the depletion region under the gate. The gate control decreases and hence the operation of MOSFET get disturbed. When the control of drain voltage is more as compared to gate voltage then channel length modulates and transistor starts conducting and its current equal to the saturation region current. This effect is more pronounced in SCE[11].

J. Quantum Mechanical Tunneling effect

The ultimate physical scaling limit of MOSFETs is direct source-to-drain tunneling. If the barrier width (transistor channel length) between source and drain becomes small enough for electrons to tunnel through the barrier without any additional gate bias, MOSFETs no longer can be used as a switch. With the continuous device scaling, the gate oxide thickness has been accordingly reduced to maintain the gate controllability over the channel. However, as the gate oxide thickness scales below 2 nm, the direct tunneling (DT) gate leakage increases exponentially due to quantum mechanical tunneling. The DT gate leakage current can not only increase standby power dissipation but also limit the proper device operation. These serious problems can be solved by replacing SiO2 with higher permittivity (high-k) gate dielectrics, which allows a physically thicker dielectric layer to have an EOT [12]. Due to the above mentioned limitations in conventional MOSFETs we moved on to the next techniques which includes the use of different device structures, different channel materials and different gate oxide materials to overcome limitation due to scaling.

III. Solution to Scaling Problem

The solution to reduce the SCE is to increase the doping. But with the increase of doping level in the channel region at the same time ionized impurities also increases and it enhanced the vertical electrical field which in turn degrade the device performance.

A. High-k Dielectric Material Gate

One of the key innovation for 25 nm process technology and beyond is the high-k/metal gate transistor, which is regarded as one of the biggest developments in transistor design in last 40 years. High-k/metal gate have enabled the continuous oxide scaling. In Si technology the value of k of silicon dioxide is 3.9. Dielectrics featuring k>3.9 are referred to as high-k dielectric while dielectric featuring k<3.9 are defined as low-k dielectrics. In cutting edge silicon nanoelectronics, both high-k and low-k dielectrics are needed to implement fully functional very high-density integrated circuit. High-k dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate) - dielectric-Si structure in MOS/CMOS transistors. Recently, high-k dielectric based on Hafnium and dual metal gate has been introduced to increase transistor performance while also reducing gate leakage as gate dielectric thickness actually increased while also the gate capacitance increased. However, such scaling cannot continue indefinitely as at certain point gate oxide will become so thin (thinner than about 1 nm) that, due to excessive tunnelling current, it would stop playing role of an insulator. Hence, dielectric featuring k higher than 3.9, i.e. one assuring same capacitive coupling. Hence, a low-k dielectric must be used to assure as little capacitive coupling between interconnect lines as possible[13].

B. Silicon-on-Insulator (SOI)

With physical separation between individual devices in high density CMOS integrated circuits measured in nanometers, proper electrical isolation between them is a key challenge. The SOI (Silicon-On-Insulator) substrate wafers, as opposed to conventional bulk wafers, not only solve the problem of electrical isolation between adjacent devices but also the reduction of the parasitic capacitances. SOI devices improved switching speed and reduced power consumption. In addition, the perfect lateral and vertical isolation from substrate provides latchup and inter-device leakage free CMOS technology. Moreover, SOI technology offers tighter transistor packing density and simplified processing [14]. SOI transistors are classified into two types; "partially depleted(PD) SOI," if the silicon film (typically 100 nm or more) on the BOX layer is thicker than the depletion region depth beneath the gate oxide, and "fully depleted (FD) SOI," if the body (silicon film) thickness is thin enough (typically 50 nm or less) or the doping concentration of the body is low enough to be fully depleted. FDSOI transistors have superior advantages over PD SOI transistors in terms of extremely low sub-threshold swing (<65 mV/decade), no floating-body effects, and low threshold voltage variation with temperature (2-3 times less). However, since FD SOI transistors are even more sensitive to process variation such as the silicon film layer variation resulting in threshold voltage fluctuation, PD SOI devices were commercially introduced first. Another important merit of SOI technology is that it provides the new device structures such as multi gate field-effect transistors (MuGFETs), which includes more than one gate into a single device. On the other hand there is a significant drawback in SOI technology. Since the BOX, which has approximately 100 times lower thermal conductivity than that of silicon, prevents thermal conduction path from SOI transistors to the substrate, SOI transistors are easily affected by the thermal heating generated in the channel, which is called Self-Heating Effects.

C. Strained Silicon Technique (S-Si)

To maintain a lower junction electric field in the channel and non-overlap of the source and drain depletion in the channel, doping becomes imperative. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel. The mobility of the charge carriers is enhanced through a concept known as the strain technology. To sum it all the benefits of strain, it results in a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility. By increasing the Ge concentration of the relaxed Si_{1-X} Ge_X substrate, the amount of biaxial strain and therefore higher magnitude of the mobility enhancement can be

achieved. Literature had confirmed a mobility enhancement factor of 2.3 for a 30% Ge concentration[16].

D. Multi Gate MOSFET

The main advantage of the multi-gate devices is to improve the short channel effects. Since the channel (body) is controlled electro statically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. This provides greater voltage gain, which is beneficial to analog circuits as well as to the noise tolerance of digital circuits. A second advantage of the multi-gate devices is the improved on-state drive current (*Ion*) and therefore faster circuit speed .As the MOS dimension has attained its physical limit, the scaling beyond 22nm node is thus an insuperable task. The improvement in device performance are obtained by multi-gate MOSFETs as they employ third dimension offering superb gate control over channel from several sides. The degree of gate controllability increases further with the quadruple-gate, the Omega/Pi-gate and the gate-all-around (GAA) structures respectively with better combinations of performance and energy efficiency [17]. As far as the characteristics lengths of the device structures are concerned, the gate-all-around MOSFETs offer the lowest characteristic length and hence the highest capability to be scaled for a given gate oxide thickness [18]. This capability gets coupled with the highest current drive per unit silicon area and demonstrates strong confinement of the electric field owing to the gate surrounding the channel.

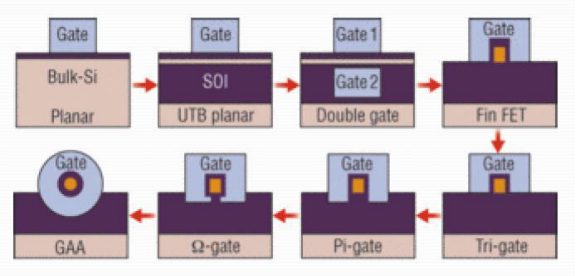

Figure 3. Progress of the MOSFET Technology through multiple-gates

E. Multi-Material Gate

One of the prominent means to reduce hot carrier effect (HCE) is using cascaded gate structure consisting of two or more metals of different work functions. This structure is commonly known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long et al. [19] or Triple-Material-Gate (TMG) in 2008 proposed by Razavi et al.[20]. The metal gates are so cascaded that the gate near the drain is a metal (M2) with lower work-function and the source side metal (M1) is of relatively higher work function. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency. Li Jin et al. described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET[21].

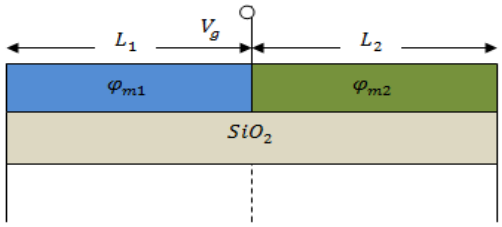

Figure 4. MOSFET Technology through multi material gates

IV. CONCLUSION AND FUTURE WORK

The integrated circuit performance increases exponentially with the scaling of MOSFET dimensions. The scaling of CMOS transistors leads to growth of semiconductor industry. In this review paper all short channel effects including their possible solution are discussed. A new device can be proposed for modeling of a SOI MOSFET using gate all around structure and multi material gate to suppressed the short channel effects. This proposed model could replace the CMOS when the scaling limit is reached to meet the today's market requirement according to ITRS.

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